

CHAPTER 5. CIRCUIT DESCRIPTION

[1] Circuit description

1. General description

The compact design of the control PWB is obtained by using ROCKWELL(CONEXANT) fax engine in the main control section and high density printing of surface mounting parts. Each PWB is independent according to its function as shown in Fig. 1.

2. PWB configuration

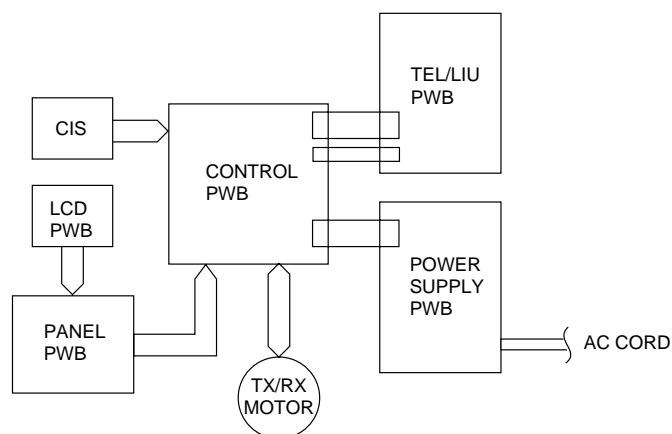


Fig. 1

1) Control PWB

The control PWB controls peripheral PWBs, mechanical parts, transmission, and performs overall control of the unit.

This machine employs a 1-chip modem (R96DFXL-CID) which is installed on the control PWB.

2) TEL/LIU PWB

This PWB controls connection of the telephone line to the unit.

3) Power supply PWB

This PWB provides voltages of +5V and +24V to the other PWBs.

4) Panel PWB

The panel PWB allows input of the operation keys.

5) LCD PWB

This PWB controls the LCD display.

3. Operational description

Operational descriptions are given below:

- Transmission operation

When a document is loaded in standby mode, the state of the document sensor is sensed via the 1 chip fax engine (FC100M). If the sensor signal was on, the motor is started to bring the document into the standby position. With depression of the START key in the off-hook state, transmission takes place.

Then, the procedure is sent out from the modem and the motor is rotated to move the document down to the scan line. In the scan processor, the signal scanned by the CIS is sent to the internal image processor and the AD converter to convert the analog signal into binary data. This binary data is transferred from the scan processor to the image buffer within the RAM and encoded and stored in the transmit buffer of the RAM. The data is then converted from parallel to serial form by the modem where the serial data is modulated and sent onto the line.

- Receive operation

There are two ways of starting reception, manual and automatic.

Depression of the START key in the off-hook mode in the case of manual receive mode, or CI signal detection by the LIU in the automatic receive mode.

First, the FC100M controls the procedure signals from the modem to be ready to receive data. When the program goes into phase C, the serial data from the modem is converted to parallel form in the modem interface of the 1 chip fax engine (FC100M) which is stored in the receive buffer of the RAM. The data in the receive buffer is decoded software-wise to reproduce it as binary image data in the image buffer. The data is DMA transferred to the recording processor within the FC100M which is then converted from parallel to serial form to be sent to the thermal head. The data is printed line by line by the FC100M which is assigned to control the motor rotation and strobe signal.

- Copy operation

To make a copy on this facsimile, the COPY key is pressed when the machine is in stand-by with a document on the document table and the telephone set is in the on-hook state.

First, depression of the COPY key advances the document to the scan line. Similar to the transmitting operation, the image signal from the CIS is converted to a binary signal in the DMA mode via the 1 chip fax engine (FC100M) which is then sent to the image buffer of the RAM. Next, the data is transferred to the recording processor in the DMA mode to send the image data to the thermal head which is printed line by line. The copying takes place as the operation is repeated.

[2] Circuit description of control PWB

1. General description

Fig. 2 shows the functional blocks of the control PWB, which is composed of 5 blocks (UX-370)/4 blocks (UX-310/FO-730).

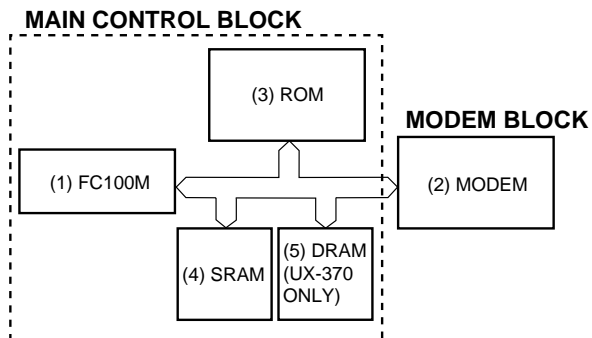


Fig. 2 Control PWB functional block diagram

2. Description of each block

(1) Main control block

UX-370: The main control block is composed of ROCKWELL (CONEXANT) 1 chip fax engine (FC100M), ROM (2Mbit), SRAM (256Kbit), DRAM (4Mbit) and Modem (R96DFXL-CID).

UX-310/FO-730:

The main control block is composed of ROCKWELL (CONEXANT) 1 chip fax engine (FC100M), ROM (2Mbit), SRAM (1Mbit) and Modem (R96DFXL-CID).

Devices are connected to the bus to control the whole unit.

1) FC100M (IC9) : pin-144 QFP (FAX CONTROLLER)

2) R96DFXL-CID (IC6) : pin-100 QFP (MODEM)

The FAXENGINE Integrated Facsimile Controllers.

FC100M, contains an internal 8 bit microprocessor with an external 2 Mbyte address space and dedicated circuitry optimized for facsimile image processing and facsimile machine control and monitoring.

3) 27C020 (IC4): pin-32 DIP (ROM)

EPROM of 2Mbit equipped with software for the main CPU.

4) W24010S-70LE (IC2): pin-32 SOP (SRAM)(UX-310/FO-730)

Line memory for the main CPU system RAM area and coding/decoding process. Used as the transmission buffer.

Memory of recorded data such as daily report and auto dials. When the power is turned off, this memory is backed up by the lithium battery.

4) W24258S-70LE (IC3): pin-28 SOP (SRAM)(UX-370)

Line memory for the main CPU system RAM area and coding/decoding process. Used as the transmission buffer.

Memory of recorded data such as daily report and auto dials. When the power is turned off, this memory is backed up by the lithium battery.

5) M514800C-70J (IC1): pin-28 SOJ (DRAM)(UX-370 ONLY)

Image memory for recording process.

- Memory for recording pixel data at without paper.

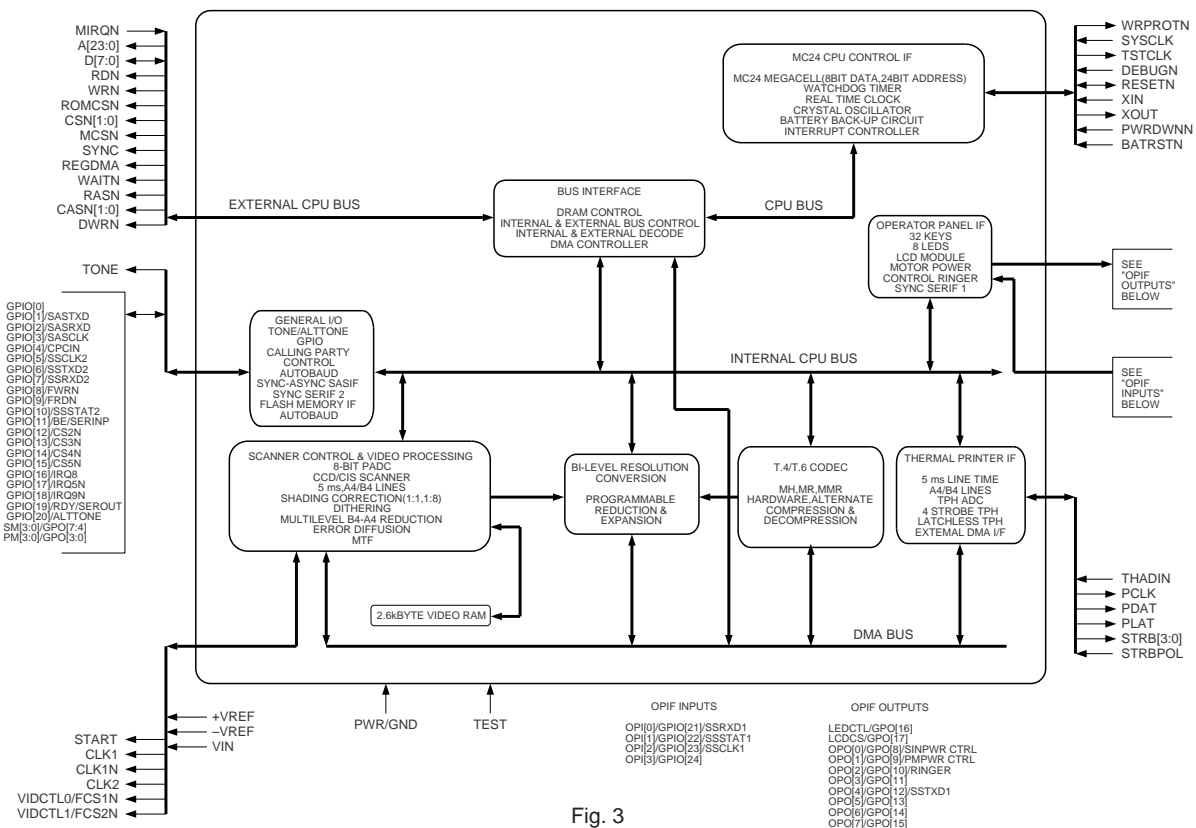


Fig. 3

FC100M (IC9) Terminal descriptions

| Pin Name | Pin No. | I/O | Input Type | Output Type | Pin Description (Note: Active low signals have an "n" pin name ending.) |
|--|-------------------------------|-----|------------|-------------|--|
| CPU Control Interface | | | | | |
| MIRQn | 135 | I | HU | – | Modem interrupt, active low. (Hysteresis In, Internal Pullup.) |
| SYSCLK | 133 | I | H | – | System clock. (Hysteresis In.) |
| TSTCLK | 130 | O | – | 123XT | Test clock. |
| Bus Control Interface | | | | | |
| A[23:0] | [1:6][8:13] [15:20][22:27] | O | TU | 123XT | Address bus (24-bit). |
| D[7:0] | [136:139] [141:144] | I/O | TU | 123XT | Data bus (8-bit). |
| RDn | 128 | O | – | 123XT | Read strobe. |
| WRn | 127 | O | – | 123XT | Write strobe. |
| ROMCSn | 120 | O | – | 123XT | ROM chip select. |
| CS1n | 122 | O | – | 123XT | I/O chip select. |
| CS0n | 57 | O | – | 123XT | SRAM chip select. (Battery powered.) |
| MCSn | 121 | O | – | 123XT | Modem chip select. |
| SYNC | 126 | O | – | 123XT | Indicates CPU op code fetch cycle (active high). |
| REGDMA | 124 | O | – | 123XT | Indicates REGSEL cycle and DMA cycle. |
| WAITn | 125 | O | – | 123XT | Indicates current TSTCLK cycle is a wait state or a halt state. |
| RASn | 113 | O | – | 123XT | DRAM row address select. (Battery powered.) |
| CAS[1:0]n | [111:112] | O | – | 123XT | DRAM column address select. (Battery powered.) |
| DWRn | 109 | O | – | 123XT | DRAM write. (Battery powered.) |
| Prime Power Reset Logic and Test | | | | | |
| DEBUGn | 129 | I | HU | – | External non-maskable input (NMI). |
| RESETn | 131 | I/O | HU | 2XO | FC100/FC200 Reset. |
| TEST | 58 | I | C | – | Sets Test mode (Battery powered). |
| Battery Power Control and Reset Logic | | | | | |
| XIN | 59 | I | OSC | – | Crystal oscillator input pin. |
| XOUT | 60 | O | – | OSC | Crystal oscillator output pin. |
| PWRDWNn | 62 | I | H | – | Used by external system to indicate -to FC100/FC200 - loss of prime power. (Results in NMI) |
| BATRSTn | 61 | I | H | – | Battery power reset input. |
| WRPROTn | 110 | O | – | 1XC | (Battery powered.) Write protect during loss of VDD power. NOTE: The functional logic is powered by battery power, but the output drive is powered by DRAM battery power. |
| Scanner Interface | | | | | |
| START | 101 | O | – | 2XS | Scanner shift gate control. |
| CLK1 | 100 | O | – | 2XS | Scanner clock. |
| CLK1n | 99 | O | – | 2XS | Scanner clock-inverted. |
| CLK2 | 98 | O | – | 2XS | Scanner reset gate control (or clock for CIS scanner). |
| FCS1n/VIDCTL0 | 96 | O | – | 2XT | Flash memory chip select or Video Control signal. |
| FCS2n/VIDCTL1 | 97 | O | – | 2XT | Flash memory chip select or Video Control signal. |
| Printer Interface | | | | | |
| PCLK/DMAACK | 29 | O | – | 3XC | Thermal Print Head (TPH) clock, or external DMAACK. |
| PDAT | 30 | O | – | 2XP | Serial printing data (to TPH). |
| PLAT | 31 | O | – | 3XP | TPH data latch. |
| STRB[3:0] | [33:36] | O | – | 1XP | Strobe signals for the TPH. |
| STRBPOL/DMAREQ | 37 | I | C | – | Sets strobe polarity, active high/low or external DMA request. |
| Operator Panel Interface | | | | | |
| OPO[0]/GPO[8]/ SMPWRCTRL | 47 | O | – | 2XL | Keyboard/LED strobe [0] or GPO[8] or Scan Motor Power Control |
| OPO[1]/GPO[9]/ PMPWRCTRL | 46 | O | – | 2XL | Keyboard/LED strobe [1] or GPO[9] or Print Motor Power Control |
| OPO[2]/GPO[10]/ RINGER | 44 | O | – | 2XCT | Keyboard/LED strobe [2] or GPO[10] or RINGER |
| OPO[3]/GPO[11] | 43 | O | – | 2XL | Keyboard/LED strobe [3] or GPO[11] |
| OPO[4]/GPO[12]/ SSTXD1 | 42 | O | – | 2XL | Keyboard/LED strobe [4] or GPO[12] or SSTXD1 (for SSIF1) |
| OPO[5]/GPO[13] | 40 | O | – | 2XL | Keyboard/LED strobe [5] or GPO[13] |
| OPO[6]/GPO[14] | 39 | O | – | 2XL | Keyboard/LED strobe [6] or GPO[14] |
| OPO[7]/GPO[15] | 38 | O | – | 2XL | Keyboard/LED strobe [7] or GPO[15] |
| OPI[0]/GPIO[21]/ SSRXD1 | 52 | I/O | HU | 2XC | (Pullup, Hysteresis In) Keyboard return [0] or GPIO[21] or SSRXD1 (for SSIF1) |
| OPI[1]/GPIO[22]/ SSSTAT1 | 51 | I/O | HU | 2XC | (Pullup, Hysteresis In) Keyboard return [1] or GPIO[22] or SSSTAT1 (for SSIF1) |

FC100M (IC9) Terminal descriptions

| Pin Name | Pin No. | I/O | Input Type | Output Type | Pin Description |
|-----------------------------------|---------------------------------------|-----|------------|-------------|--|
| Operator Panel Interface | | | | | |
| OPI[2]/GPIO[23]/SSCLK1 | 50 | I/O | HU | 2XC | (Pullup, Hysteresis In) Keyboard return [2] or GPIO[23] or SSCLK1 (for SSIF1) |
| OPI[3]/GPIO[24] | 49 | I/O | HU | 2XC | (Pullup, Hysteresis In) Keyboard return [3] or GPIO[24] |
| LEDCTL | 55 | O | – | 4XC | Indicates outputs OPO[7:0] are for LEDs. |
| LCDCS | 54 | O | – | 1XC | LCD chip select. |
| General Purpose I/O | | | | | |
| GPIO[0] | 94 | I/O | H | 2XC | (Hysteresis In) GPIO[0]. |
| GPIO[1]/SASTXD | 93 | I/O | H | 2XC | (Hysteresis In) GPIO[1] or SASTXD (for SERIF). |
| GPIO[2]/SASRXD | 92 | I/O | H | 2XC | (Hysteresis In) GPIO[2] or SASRXD (for SERIF). |
| GPIO[3]/SASCLK | 91 | I/O | H | 2XC | (Hysteresis In) GPIO[3] or SASCLK (for SERIF). |
| GPIO[4]/CPCIN | 90 | I/O | H | 2XC | (Hysteresis In) GPIO[4] or Calling Party Control Input. |
| GPIO[5]/SSCLK2 | 89 | I/O | H | 2XC | (Hysteresis In) GPIO[5] or SSCLK2 (for SSIF2). |
| GPIO[6]/SSTXD2 | 87 | I/O | H | 2XC | (Hysteresis In) GPIO[6] or SSTXD2 (for SSIF2). |
| GPIO[7]/SSRXD2 | 86 | I/O | H | 2XC | (Hysteresis In) GPIO[7] or SSRXD2 (for SSIF2). |
| GPIO[8]/FWRn | 85 | I/O | H | 2XC | (Hysteresis In) GPIO[8] or flash write enable signal for NAND-type flash memory. |
| GPIO[9]/FRDn | 84 | I/O | H | 2XC | (Hysteresis In) GPIO[9] or flash read enable signal for NAND-type flash memory. |
| GPIO[10]/SSSTAT2 | 83 | I/O | H | 2XC | (Hysteresis In) GPIO[10] or SSSTAT2 (for SSIF2). |
| GPIO[11]/BE/SERINP | 82 | I/O | H | 1XC | (Hysteresis In) GPIO[11] or bus enable or serial port data input for autobaud detection. |
| GPIO[12]/CS[2]n | 80 | I/O | H | 2XC | (Hysteresis In) GPIO[12] or I/O chip select [2]. |
| GPIO[13]/CS[3]n | 79 | I/O | H | 2XC | (Hysteresis In) GPIO[13] or I/O chip select [3]. |
| GPIO[14]/CS[4]n | 78 | I/O | H | 2XC | (Hysteresis In) GPIO[14] or I/O chip select [4]. |
| GPIO[15]/CS[5]n | 77 | I/O | H | 2XC | (Hysteresis In) GPIO[15] or I/O chip select [5]. |
| GPIO[16]/IRQ[8] | 76 | I/O | H | 1XC | (Hysteresis In) GPIO[16] or external interrupt 8. |
| GPIO[17]/IRQ[5]n | 75 | I/O | H | 1XC | (Hysteresis In) GPIO[17] or external interrupt 5. |
| GPIO[18]/IRQ[9]n | 74 | I/O | H | 1XC | (Hysteresis In) GPIO[18] or external interrupt 9. |
| GPIO[19]/RDY/SEROUT | 73 | I/O | H | 1XC | (Hysteresis In) GPIO[19] or ready signal or Serial port data output for autobaud detection. |
| GPIO[20]/ALTTONE | 107 | I/O | H | 1XC | (Hysteresis In) GPIO[20] or ALTTONE. |
| Miscellaneous | | | | | |
| SM[3:0]/GPO[7:4] | [103:106] | O | – | 1XC | Programmable: scan motor control pins or GPO pins. |
| PM[3:0]/GPO[3:0] | [115:118] | O | – | 1XC | Programmable: print motor control pins or GPO pins. |
| TONE | 119 | O | – | 1XC | Tone output signal. |
| Power, Reference Voltages, Ground | | | | | |
| -Vref/CLREF | 66 | I | -VR | – | Negative Reference Voltage for Video A/D or Reference Voltage for the Clamp Circuit. |
| ADXG | 68 | I | VXG | – | A/D Internal GND. (NOTE: This pin requires an external 0.22µF decoupling capacitor to ADGA.) |
| ADGA | 69 | | VADG | | A/D Analog Ground |
| ADVA | 70 | | VADV | | A/D Analog Power |
| ADGD | 72 | | VADG | | A/D Digital Ground |
| +Vref | 71 | I | +VR | | Positive Reference Voltage for Video A/D. |
| VIN | 67 | I | VA | – | Analog Video A/D input. |
| THADI | 65 | I | TA | – | Analog Thermal A/D input. |
| Power and Ground | | | | | |
| VSS(12) | 7,21,28,45,53,56,64,88,95,108,132,134 | | | | Digital Ground |
| VDD(8) | 14,32,41,48,81,102,123,140 | | | | Digital Power |
| VBAT | 63 | | | | Battery Power |
| VDRAM | 114 | | | | DRAM Battery Power |

(2) Panel control block

The following controls are performed by the FC100M.

- Operation panel key scanning
- Operation panel LCD display

(3) Mechanism/recording control block

- Recording control block diagram (1)

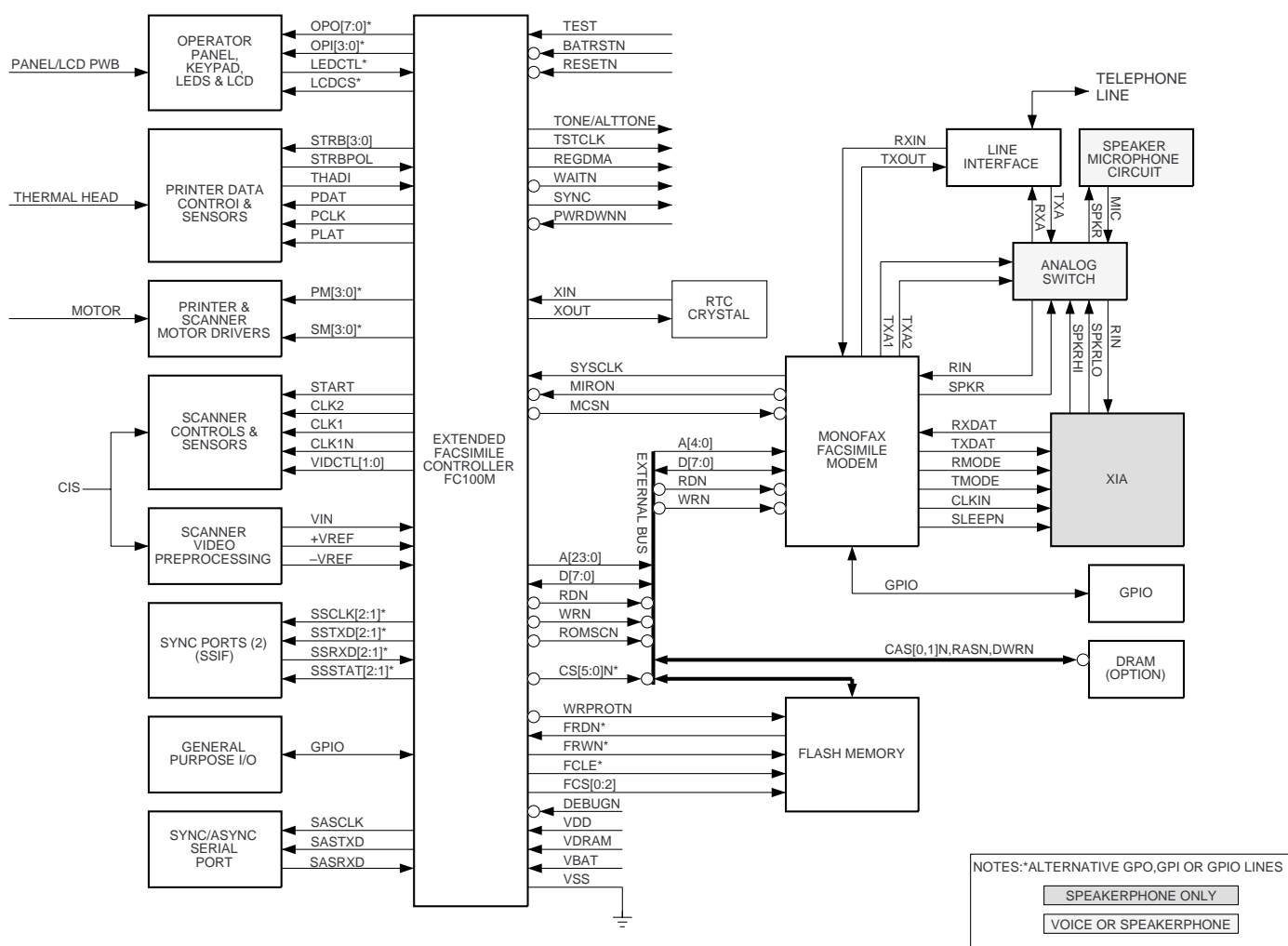


Fig. 4

(4) Modem (R96DFXL-CID) block

INTRODUCTION

The ROCKWELL(CONEXANT) R96DFXL-CID MONOFAX modem is a synchronous 9600 bits per second (bps) half-duplex modem with error detection and DTMF reception. It has low power consumption and requires only a single +5V DC power supply. The modem is housed in a single VLSI device package.

The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The R96DFXL-CID is designed for use in Group 3 facsimile machines. The modem satisfies the requirements specified in CCITT recommendations V.29, V.27 ter, V.21 Channel 2 and T.4, and meets the binary signaling requirements of T.30.

The modem can operate at 9600, 7200, 4800, 2400, or 300 bps, and also includes the V.27 ter short training sequence option.

The modem can also perform HDLC framing according to T.30 at 9600, 7200, 4800, 2400, or 300 bps.

The modem features a programmable DTMF receiver and three programmable tone detectors which operate concurrently with the V.21 channel 2 receiver.

The voice mode allows the host computer to efficiently transmit and receive audio signals and messages.

The modem is available in either a 100-pin plastic quad flat pack (PQFP) or a 64-pin quad in-line package (QUIP).

General purpose input/output (GPIO) pins are available for host as signment in the 100-pin PQFP.

The modem's small size, single voltage supply, and low power consumption allow the design of compact system enclosures for use in both office and home environments.

MONOFAX is a registered trademark of ROCKWELL(CONEXANT) International.

FEATURES

- Group 3 facsimile transmission/reception
 - ITU-TS V.29, V.27 ter, T.30, V.21 Channel 2, T.4
 - HDLC Framing at all speeds
- V.27 ter short train
- Concurrent DTMF, FSK, and tone reception
- Voice mode transmission/reception
- Half-duplex (2-wire)
- Programmable maximum transmit level:
 - 0 dBm to –15 dBm
- Programmable transmit analog attenuation:
 - 0 dB to 14 dB in 2 dB steps
- Receive dynamic range: 0 dBm to –43 dBm
- Programmable dual tone generation
- Programmable tone detection
- Programmable turn-on and turn-off thresholds
- Programmable interface memory interrupt
- Diagnostic capability
 - Allows telephone line quality monitoring
- Equalization
 - Automatic adaptive equalizer
 - Fixed digital compromise equalizer
- DTE interface: two alternate ports
 - Selectable microprocessor bus (6500 or 8085)
 - CCITT V.24 (EIA-232-D compatible) interface
- TTL and CMOS compatible
- Low power consumption: 275 mW (typical)
- Single Package
 - 100-pin PQFP
 - 64-pin QUIP
- Single +5VDC power supply
- Software compatible with R96MFX, R96EFX, R96SHF, and R96VFX modems

R96DFXL-CID (IC6) Hardware Interface Signals

Pin Signals – 100-Pin PQFP

| Pin No. | Signal Name | I/O Type |
|---------|-------------|----------|
| 1 | GP03 | IA/OB |
| 2 | GP04 | IA/OB |
| 3 | GP05 | IA/OB |
| 4 | GP06 | IA/OB |
| 5 | GP07 | IA/OB |
| 6 | 0VD2 | GND |
| 7 | 0VD2 | GND |
| 8 | D7 | IA/OB |
| 9 | D6 | IA/OB |
| 10 | D5 | IA/OB |
| 11 | D4 | IA/OB |
| 12 | D3 | IA/OB |
| 13 | D2 | IA/OB |
| 14 | D1 | IA/OB |
| 15 | D0 | IA/OB |
| 16 | 0VD2 | GND |
| 17 | 0VA | GND |
| 18 | RAMPIN | R |
| 19 | NC | |
| 20 | NC | |
| 21 | 0VA | GND |
| 22 | +5VD2 | PWR |
| 23 | 0VD1 | GND |
| 24 | SWGAINI | R |
| 25 | ECLKIN1 | R |
| 26 | SYNCIN1 | R |
| 27 | NC | |
| 28 | NC | |
| 29 | NC | |
| 30 | 0VA | GND |
| 31 | NC | |
| 32 | NC | |
| 33 | NC | |
| 34 | DAIN | R |
| 35 | ADOUT | R |
| 36 | BYPASS | IC |
| 37 | RCVI | R |
| 38 | TXLOSS3 | IC |
| 39 | TXLOSS2 | IC |
| 40 | TXLOSS1 | IC |
| 41 | NC | |
| 42 | NC | |
| 43 | 0VA | GND |
| 44 | TXOUT | AA |
| 45 | RXIN | AB |
| 46 | +5VA | PWR |
| 47 | 0VA | GND |
| 48 | AGD | R |
| 49 | AOUT | R |
| 50 | 0VD1 | GND |
| 51 | NC | |
| 52 | IRQ | OC |
| 53 | WRITE-R/W | IA |
| 54 | CS | IA |
| 55 | READ-φ2 | IA |
| 56 | RS4 | IA |
| 57 | RS3 | IA |
| 58 | RS2 | IA |
| 59 | RS1 | IA |

| Pin No. | Signal Name | I/O Type |
|---------|-------------|----------|
| 60 | RS0 | IA |
| 61 | GP13 | IA/OB |
| 62 | NC | |
| 63 | GP11 | IA/OB |
| 64 | RTS | IA |
| 65 | EN85 | R |
| 66 | 0VD2 | GND |
| 67 | PORI | ID |
| 68 | XTLI | R |
| 69 | XTLO | R |
| 70 | XCLK | OD |
| 71 | YCLK | OD |
| 72 | +5VD1 | PWR |
| 73 | DCLK1 | R |
| 74 | SYNCIN2 | R |
| 75 | GP16 | IA/OB |
| 76 | GP17 | IA/OB |
| 77 | 0VD2 | GND |
| 78 | CTS | OA |
| 79 | TXD | IA |
| 80 | 0VD2 | GND |
| 81 | 0VD2 | GND |
| 82 | DCLK | OA |
| 83 | EYESYNC | OA |
| 84 | EYECLKX | OA |
| 85 | EYECLK | OA |
| 86 | EYEX | OA |
| 87 | ADIN | R |
| 88 | DAOUT | R |
| 89 | 0VD2 | GND |
| 90 | EYEX | OA |
| 91 | GP21 | IA/OB |
| 92 | 0VD2 | GND |
| 93 | GP20 | IA/OB |
| 94 | GP19 | IA/OB |
| 95 | RXD | OA |
| 96 | RLSD | OA |
| 97 | 0VD2 | GND |
| 98 | RCVO | R |
| 99 | SWGAINO | R |
| 100 | GP02 | IA/OB |

Notes:

1. NC = No connection; leave pin disconnected (open).
2. I/O Type: = Digital signals: see Table 9;
Analog signals: see Table 10.
3. R = Required modem inter-connection; no connection to host equipment.

2. Line filter block

This block is comprised of coil L2.

3. Dial pulse generation circuit

The pulse dial generation circuit comprises of transistor Q1, the photo-coupler PC5, PC9, and zener diode ZD8.

Dial pulses supplied from CPU are amplified by transistor Q1 through a photo-coupler PC9 to the telephone line.

4. On-hook circuit

This circuit comprises of CML relay and switch SW2, and CML and SW2 are for connection of the telephone line.

5. Matching transformer

The matching transformer performs electrical insulation from the telephone line and impedance matching for transmitting the TEL/FAX signal.

6. Hybrid circuit

The hybrid circuit performs 2-wire-to-4-wire conversion using the IC101 of operational amplifier, transmits the voice transmission signal to the line, and feeds back the voice signal to the voice reception circuit as the side tone.

7. Signal selection

The following signals are used to control the transmission line of TEL/LIU signal. For details, refer to the signal selector matrix table.

8. Sensor circuit

For the recording paper sensor (P-E, P-IN), when there is recording paper, the photo transistor in the light receiving side is ON and the detection level is LOW. When there is no recording paper, the photo transistor in the light receiving side is OFF and the detection level is HIGH.

9. CI detection circuit

The CI detection circuit detects the CI signals. A CI signal, which is provided to the photo-coupler PC10 through the C9 (1.8 μ F), R4 (10 K), and ZD2 when the ring signal is inputted from the telephone line.

10. Power supply and bias circuits

The voltages of +5V and +24VA are supplied from the control PWB unit.

[Control signals from output port]

| Signal Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|-------|-------|--------------------|--------|--------------------|--------|------|--|---|---|---|-----|---|-----|--|---|---|---|--------|-------|--------|--|---|---|---|------|---|------|
| CML (The circuit is located in the TEL/LIU PWB.) | <u>Line connecting relay and DP generating relay</u> H: Line make L: Line break | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SP MUTE | <u>Speaker tone mute control signal</u> H: Muting (Power down mode) L: Muting cancel (Normal operation) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RX MUTE | <u>Handset reception mute control signal</u> H: Muting L: Muting cancel | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DP ON | <u>DP generating relay</u> H : DP break L : DP make | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VOL A VOL B VOL C (The circuit is located in the control PWB.) | <u>Speaker volume control signal</u> VRSEL1 VRSEL2 matrix <table border="1"> <thead> <tr> <th></th> <th>VOL A</th> <th>VOL B</th> <th>VOL C</th> <th>RING/ Receiving</th> <th>Buzzer</th> <th>DTMF</th> </tr> </thead> <tbody> <tr> <td></td> <td>L</td> <td>L</td> <td>L</td> <td>Low</td> <td>—</td> <td>Low</td> </tr> <tr> <td></td> <td>H</td> <td>L</td> <td>L</td> <td>Middle</td> <td>Fixed</td> <td>Middle</td> </tr> <tr> <td></td> <td>L</td> <td>L</td> <td>H</td> <td>High</td> <td>—</td> <td>High</td> </tr> </tbody> </table> | | VOL A | VOL B | VOL C | RING/ Receiving | Buzzer | DTMF | | L | L | L | Low | — | Low | | H | L | L | Middle | Fixed | Middle | | L | L | H | High | — | High |
| | VOL A | VOL B | VOL C | RING/ Receiving | Buzzer | DTMF | | | | | | | | | | | | | | | | | | | | | | | |
| | L | L | L | Low | — | Low | | | | | | | | | | | | | | | | | | | | | | | |
| | H | L | L | Middle | Fixed | Middle | | | | | | | | | | | | | | | | | | | | | | | |
| | L | L | H | High | — | High | | | | | | | | | | | | | | | | | | | | | | | |
| TXCONT (The circuit is located in the control PWB.) | <u>Handset transfer mute control signal</u> H: Signal sending, when transmitting L: During reception, transmission mute, (during standby) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GAIN-C (The circuit is located in the control PWB.) | <u>Reception gain switching signal</u> H: When connected to line, 1: 1 gain L: When not connected to line, HIGH gain | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BZCONT (The circuit is located in the control PWB.) | <u>Speaker output signal switching</u> H: Buzzer signal output L: When monitoring line signal | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

[Signals for status recognition according to input signals]

| Signal Name | Function |
|-------------|--|
| RHS | H: The handset is in the on-hook state. L: The handset is in the off-hook state. |
| CI | Incoming call (CI) detection signal |
| P-E | H: Recording paper does not exist. L: Recording paper is set (exists). (Detection of recording paper in printing state) |
| P-IN | H: Recording paper does not exist in case of printing. L: Recording paper exists in case of printing. (Detection of recording paper in printing state) |

| NO | Signal Name (CNLIUA) | NO | Signal Name (CNLIUA) |
|----|----------------------|----|----------------------|
| 1 | TELMUTE | 7 | RXIN |
| 2 | CI/CIDIN1 | 8 | TXOUT |
| 3 | CIDIN2/HS | 9 | CML |
| 4 | P-E | 10 | +5V |
| 5 | P-IN | 11 | DG |
| 6 | RHS | 12 | +24VA |

| NO | Signal Name (CNLIUB) | NO | Signal Name (CNLIUB) |
|----|----------------------|----|----------------------|
| 1 | EXTSIG | 4 | DPON |
| 2 | RLYCNT | 5 | DPMUTE |
| 3 | SIGMUTE/TXMUTE | 6 | E-RLY |

[Other signals]

| Signal Name | Function |
|-------------|---|
| TXOUT | Transmission (DTMF) analog signal output from modem |
| RXIN | Reception (DTMF, others) analog signal input into modem |

(Example: TEL speaking)

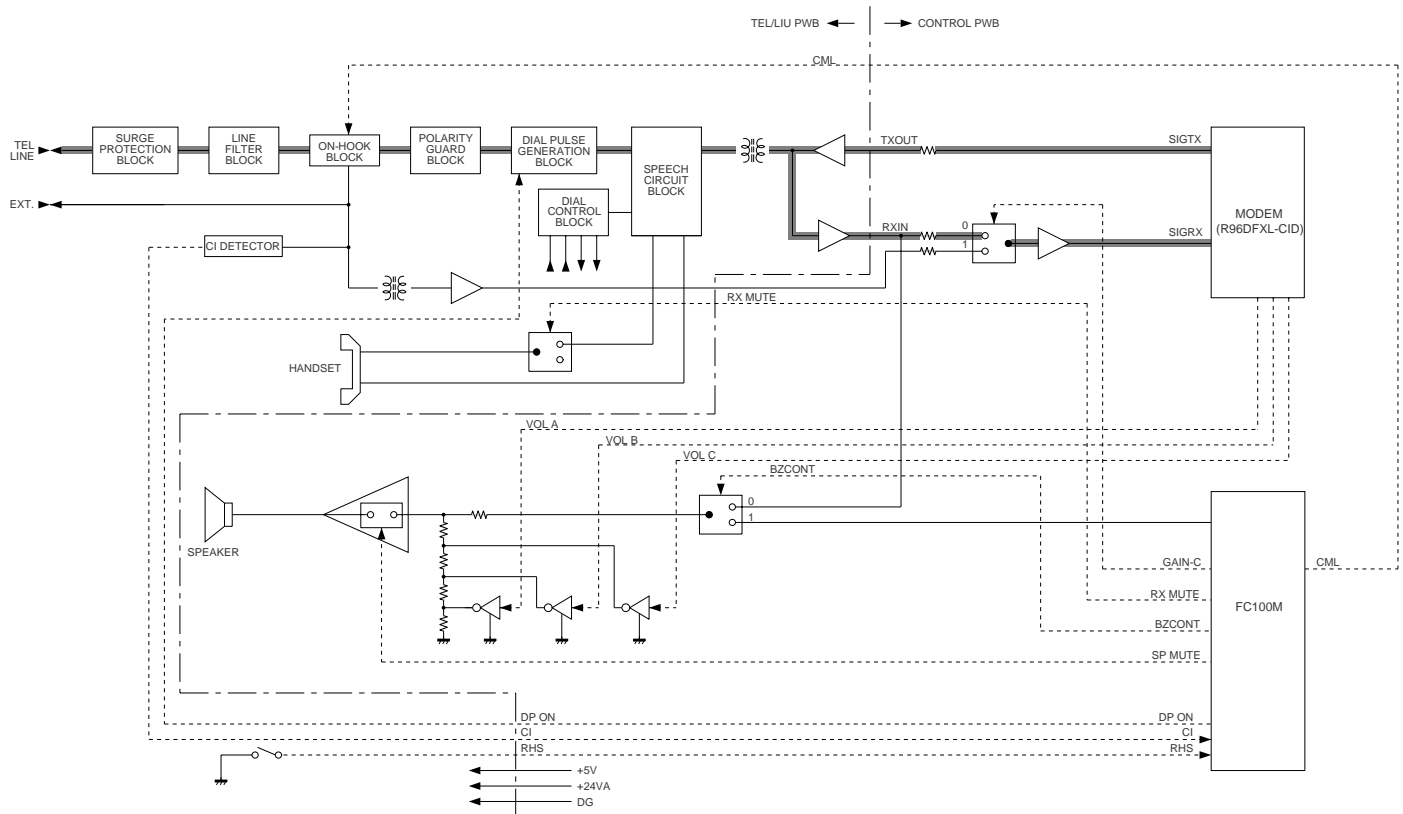


Fig. 6

[4] Circuit description of power supply PWB

1. Block diagram

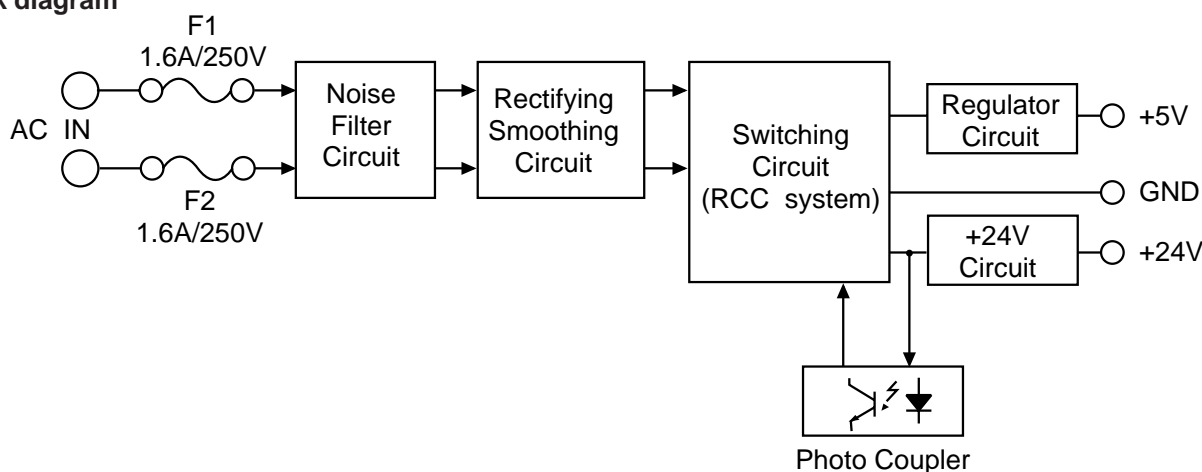


Fig. 7

2-1. Noise filter circuit

The input noise filter section is composed of L1, C1 and C15 that reduces normal mode noise from the AC line and common mode noise to the AC line.

2-2. Rectifying/smoothing circuit

The AC input voltage is rectified by diode D1, 2, 3, 4 and smoothed by capacitor C2 to supply DC voltage to switching circuit section.

Power thermistor TH1 suppresses inrush current at power switch-on.

2-3. Switching circuit

This circuit employs the self excited ringing choke convertor (RCC) system. In this system, the DC voltage supplied from the rectifying/smoothing section is converted to be the high frequency pulses by ON/OFF repetition of MOS FET Q1.

Energy is charged in the primary winding of T1 during ON period of Q1, and discharged to the secondary winding during OFF period of Q1.

The output voltage is controlled by adjusting ON period of Q1 which changes charge time of C8 through operation of photo-coupler PC1 from +24V output.

The overcurrent protection is performed by bringing Q1 to OFF state through detection of voltage increase in the auxiliary winding of T1 by ZD2, R5 and R6.

The overvoltage protection is performed by operating the overcurrent protection circuit through destruction of zener diode ZD4 and short-circuiting of load.

2-4. +5V circuit

Each DC voltage supplied by rectifying the output of transformer T1 with diode D8 is stabilized by 3-terminal regulator IC1.

[5] Circuit description of CIS unit

1. CIS

Cis is an image sensor which puts the original paper in close contact with the full-size sensor for scanning, being a monochromatic type with the pixel number of 1,728 dots and the main scanning density of 8 dots/mm.

It is composed of sensor, rod lens, LED light source, light-conductive plate, control circuit and so on, and the reading line and focus are previously adjusted as the unit.

Due to the full-size sensor, the focus distance is so short that the set is changed from the light weight type to the compact type.

2. Waveforms

The following clock is supplied from FC100M of the control board, and VO is output.

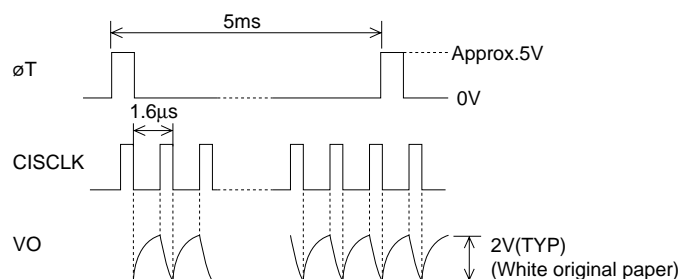


Fig. 8